forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

depositing a buffering layer over the semiconductor substrate, including the gate pattern and the lightly doped regions;

forming sidewall spacers on a portion of the buffering layer at both sidewalls of the gate pattern to produce a gate structure;

injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

removing an exposed portion of the buffering layer to expose upper surfaces of the heavily doped regions and the polysilicon gate;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped region.

10. (New) The method according to claim 9, wherein the buffering layer is a SiO_2 layer.

11. (New) The method according to claim 9, wherein the buffering layer is a SiN layer.

12. (New) The method according to claim 9, wherein the thickness of buffering layer is about 30Å or more.

13. (New) The method according to claim 9, wherein the transition metal is made of at least one selected from a group consisting group of Co, Ti, Ni.

14. (New) A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

depositing a buffering layer over the semiconductor substrate, including the gate pattern and the lightly doped regions;

forming sidewall spacers on a portion of the buffering layer at both sidewalls of the gate pattern to produce a gate structure;

injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

removing an exposed portion of the buffering layer to expose upper surfaces of the heavily doped regions and the polysilicon gate.

15. (New) The method according to claim 14, wherein the buffering layer is a SiO_2 layer.

16. (New) The method according to claim 14, wherein the buffering layer is a SiN layer.